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Internationalisation of Innovation: Why is Chip Design Moving to Asia?

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Internationalisation of Innovation: Why is Chip Design Moving to Asia?[1]
by
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East West Center, Honolulu, Hawaii, USA
24 March, 2004

Introduction

One of Keith Pavitt's many contributions to the study of innovation is the proposition that physical proximity is advantageous for innovative activities that involve highly complex technological knowledge, uncertainty, and coordinated experimentation across functional and disciplinary boundaries (Pavitt, 1999: XI). This description precisely captures the nature of chip design, a process that creates the greatest value in the electronics industry. Pavitt distinguishes cognitive and organizational dimensions of technological complexity. As for the cognitive dimension, an artifact like a chip is "made up of numerous components and subsystems whose interactions are often non-linear and therefore impossible to predict" (Pavitt, 1999: p.X). Verification and testing become critical bottlenecks. Hence tacit knowledge is central for interpreting the performance of a chip, and for "knowing how and where to search for improved performance" (ibid). The organizational dimension of technological complexity implies that "…a wide and increasing range of fields of specialized knowledge are being mobilized…", which necessitates "linkages with the wider knowledge communities and the capacity within the firm to experiment and learn across cognitive and functional boundaries" (Pavitt, 1999: pages X and XI).

One would thus expect chip design to be spatially immobile, much less prone than manufacturing to geographic relocation. Until quite recently, chip design has indeed remained heavily concentrated, both geographically and organizationally. Geographically, chip design was restricted to a few centers of excellence, mainly in the US, but also in Europe and Japan. Organizationally, three types of firms dominated chip design: system companies (like IBM or Philips) that are captive chip producers; integrated device manufacturers (like Intel) that produce high-volume integrated circuits (ICs); and "fabless" chip design houses (like Xilinx or Altera) that target specialized niche markets. However, fundamental changes have occurred over the last few years in the location of chip design that are signaling a growing mobility. Of particular importance has been a massive geographic dispersion of chip design to leading Asian electronics exporting countries. Taiwan has emerged as a primary new location, with Korea following closely behind, and chip design is rapidly growing in China and India, as well as in Singapore and Malaysia.

This paper explores why chip design is moving to Asia, despite its high knowledge-intensity. I distinguish "pull" and "push" factors. "Pull" factors are differences in the cost of employing a chip design engineer across locations that result from comparative factor and resource advantages, and from support policies that provide incentives and "public goods"[2]. Pull factors are important - they explain what attracts chip design to particular locations. However, they cannot explain under what conditions physical proximity can become a disadvantage rather than an advantage for innovative activities that involve highly complex technological knowledge. A

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[1] This paper draws on discussions with the late Keith Pavitt, as part of an email correspondence on his manuscript "Are systems designers & integrators "post-industrial" firms?" (Pavitt, 2003 a) during the fall of 2002. The author gratefully acknowledges comments and suggestions from William Lazonick, Mike Hobday, Norio Tokumaru, Stefano Brusoni, David Levy , Boy Luethje, Shin-Horng Chen, AnnoLee Saxenian, Ismail Zawawi, Anna Ong, Grant Martin, Barry Naughton,

[2] For instance, chips designed by foreign and domestic companies in China are eligible for a 14% VAT tax rebate, which lowers the effective tax rate to 3%, from the nominal VAT of 17% on sales of imported and domestically produced chips (iSupply, 2003: 41, quoting State Circular # 18, amended in September 2001). This policy obviously creates a powerful artifical cost advantage for domestically designed chips.

central proposition of this paper is that Pavitt's conceptualization of cognitive and organizational complexity can help to explain what forces are behind the growing geographic mobility of chip design, pushing for and enabling its dispersion to Asia[3].

Specifically, I argue that chip design is moving to Asia in response to radical changes in design methodology ("system-level integration" through "modular design") and organization (automated "design factory"*). Both changes have been introduced to improve design productivity and to cope with growing complexity at two levels of chip design: on the chip ("silicon") and on the "system"[4]. However, as so often happens in the history of innovation, *de facto* impacts fail to match with expectations. We will see that both changes in methodology and organization have further increased the cognitive and organizational complexity of design. As a result, it is now less likely that a single company will exclusively handle all stages of design for a specific chip. Instead, many companies are contributing, based upon their specific areas of expertise. In short, *integrated* forms of design organization, where (almost) entire ICs are designed within a single firm, are giving way to *vertical specialization* where stages of chip design are outsourced to other firms (*dis-integration of firm organization*) and relocated across national boundaries (*geographic dispersion*).

But vertical specialization does not imply that the "Visible Hand" of large global corporations will become invisible (as argued, for instance, in Langlois, 2001), giving rise to a resurgence of market forces[5]. I will show that network integration is the necessary complement to vertical specialization[6]. Global corporations (the "network flagships") integrate geographically dispersed companies (the "network suppliers") that are contributing to the complete solution of a particular chip design project into hierarchical *global design networks* (GDNs)[7]. Vertical specialization increases the number and variety of network participants, as well as the variety of business models, which in turn increases the organizational complexity of these networks. The main purpose of GDNs is to facilitate the reuse of design building blocks, the so-called "silicon intellectual properties" (SIPs). Hence, knowledge-sharing is the glue that keeps these networks growing.

These propositions are based on interviews that I conducted during 2002 and 2003 with a sample of 60 companies and 15 research institutions that are involved in chip design in Taiwan, Korea, China and Malaysia. The sample includes ten *strategic groups* of firms (both global and regional players) that participate in GDNs: system companies; integrated device manufacturers (IDMs); providers of electronic manufacturing services (EMSs) and design services (the so-called ODMs, or "original-design-manufacturers"); "fabless" chip design houses; "chipless" licensors of "silicon intellectual properties" (SIPs); chip contract manufacturers ("foundries"); vendors of electronic design automation (EDA) tools; chip packaging and testing companies; and

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[3] In a companion paper, Ernst (forthcoming b), I will examine the role that Asian government policies and public institutions have played in fostering and upgrading local design capabilities.

[4] "Silicon complexity" refers to malfunctions that result from the growing scale and density of the circuit and the introduction of new materials or design architectures. "System complexity" on the other hand increases with the transition to system-level design with "exploding" multiple functions, like in smart phones (ITRS, 2002: 82,83).

[5] For a robust critique, see Pavitt, 2003b, Brusoni, 2003, and Tokumaru, 2003. See also van Assche, 2003, who demonstrates that vertical specialization may co-exist with re-integration through hierarchical cross-border corporate networks, using an industry-equilibrium model with monopolistic competition and perfect contracts.

[6] For the underlying conceptual framework, see Ernst (1997, 2002a, 2002b, 2003a, and 2003c).

[7] A focus on vertical specialization *within* GDNs distinguishes this paper from Linden and Somaya (2003) who juxtapose "integrated" and "licensing" modes of design organization to compare their relative transaction costs. While that article contains many interesting observations, the authors get trapped by their narrow focus on the "hierarchy-versus-network" dichotomy.

design implementation service providers; and institutes and universities (both private and public)[8].

To tell this story, I proceed in four steps. Part 1 reviews evidence on the evolution of chip design to Asia, to establish what stages and capabilities have been dispersed to this region, and who are the main carriers of design relocation. The rest of the paper explores how changes in the methodology and organization of chip design have increased both cognitive and organizational complexity, and why this facilitates the relocation of design to new, lower-cost locations in Asia. In part 2, I will examine how intensifying pressures to improve design productivity, combined with increasingly demanding performance requirements for electronic systems have produced an upheaval in design methodology, the so-called "system-on-chip" (SoC) revolution"[9]. In part 3, I will explore attempts to adjust the organization of design, so that the new methodologies can produce the expected results. Specifically, I will look at changes in skill requirements and work organization and at attempts to reduce the so-called behavioral and cultural barriers (or in plain words: resistance) to the reuse of design knowledge. Part 4 asks why vertical specialization takes place within GDNs. I demonstrate that these networks are necessary to manage multiple design interfaces that reflect the growing complexity of SoC design. I also highlight enabling forces that are gradually reducing constraints to the diffusion of chip design to Asia.

1. Evolution of Chip Design in Asia

The emergence of East Asia as a global export manufacturing base during the last decades of the late 20th century is one of the few success stories of Third World industrialization[10]. In electronic hardware manufacturing for instance, five Asian countries (China, Korea, Taiwan, Singapore and Malaysia) account for over one quarter of world production. Furthermore, while India has failed to excel as a global manufacturing exporter, the country has firmly established itself as a global export production base for software and information services.

Over the last few years, something new has happened. In the midst of a global downturn in the electronics industry, Asia's leading exporting countries appear to have seized upon new opportunities to create commercially successful innovations in the production of hardware, software, and services (Amsden and Tschang, 2003; Ernst, 2003 b and 2004a). Of particular importance are attempts to enter the global market for chip design. These attempts are poorly understood and under-researched.

All standard data sources for the global chip design industry[11] confirm that a massive relocation of electronics design is under way to the above Asian countries. For instance, Asia

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[8] In China, the firm sample includes state-owned enterprises (SOEs), collective enterprises, and private technology firms.

[9] See the titles of two influential chip design text books that document the basic principles and the evolution of SoC design: "Surviving the SOC Revolution…" (Chang et al, 1999) and "Winning the SoC Revolution" (Martin. and H. Chang, eds., 2003) .

[10] e.g., Hobday, 1995; Mathews and Cho, 2000; Amsden and Chu, 2003; Ernst and O'Connor, 1992; Ernst, Ganiatsos and Mytelka, 1998; Ernst, 2000.

[11] The paper draws on the following data sources: interviews with the sample of companies described above; various editions of the International Technology Roadmap for Semiconductors (ITRS), published by the US Semiconductor Industry Association, together with the associations of Japan, Korea, Taiwan and Europe (especially ITRS 2002 and 2004); commercial consulting surveys, prepared by Gartner/Dataquest, the Electronic Engineering Times, iSuppli, and IBS; company reports (e.g. 10K, 20F, Datamonitor, etc); and reports and data provided by public research institutes and support institutions in the US and the above Asian countries . In *China*, this includes the China Centre for Information Industry Development (CCID) at the Ministry of Information Industry; the Ministry of Science & Technology; the Shanghai Research Center for Integrated Circuit Design, and Science Park policy planning departments in Beijing, Shanghai, Suzhou, Hangzhou and Nanjing. In *Taiwan*, this includes the Institute for Information Industry (III), relevant divisions of the Industrial Technology Research Institute (ITRI), e.g., the Electronic Research & Service Organization and the System-on-Chip Technology Center, as well as such

(excluding Japan) is the fastest growing market for EDA (= electronic design automation) tools, growing 24% in 2000, compared with 6% growth in North America, 13 % in Europe, and 17% in Japan (iSuppli, 2001). A survey conducted in January 2003 suggests that, excluding Japan, Asia's share in the global production of chip designs has increased from practically nothing during the mid 1990s to around 30% in 2002, relative to North America's share of 60% (iSuppli, 2003: 21). Over the five years until 2008, Asia's share is projected to grow to more than 50%. Such projections are in line with a widespread consensus in the industry, confirmed in the author's interviews, that "the center of gravity of the global semiconductor industry … (is rapidly shifting, DE) …to the Asia-Pacific region "[12], primarily centered on "Greater China", Korea and India.

1.1. Stages of Design

But such broad-brush figures tell us little about what stages of design are involved, and who are the main carriers of design relocation. Based on a widely used flow chart for chip design, Chang and Tsai (2002) provide a useful classification into "system/application specification" (the three shaded boxes in the upper part of the figure) and "design implementation" (the six boxes in the middle of the figure that are un-shaded) (see **Figure 1**). I use this distinction to highlight two important features of chip design in Asia. First, it has a much longer history in Asia than is generally known. And, second, while design implementation has played a dominant role, system specification has started to gain in importance over the last few years.

Figure 1: Taiwan's Competitive Advantage in Digital Circuit Design

Note however that the distinction between design implementation and system specification cannot be used to distinguish design stages by knowledge complexity. Of course, system specification provides leverage for defining global standards and for innovation rents via premium pricing. However, as will be explained below, it does not necessarily require more complex knowledge than design implementation. Knowledge complexity depends on how much functionality is squeezed onto the chip, the printed circuit board, or the system. Equally important is the sophistication of the design methodology. Knowledge complexity tends to increase substantially for the six design implementation stages, the closer chip design is moving from the individual component to system-level integration, and the greater use is made of "modular design".

1.2. History: Carriers of Asian Chip Design

Electronic design in Asia started during the early 1980s with board-level design performed in Asian computer and consumer electronics companies (primarily in Korea and Taiwan) to provide the optimum in the circuit layout of discrete components (including ICs, capacitors, inductors,

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institutions as the National SOC Research Program (Si-Soft) at the National Chiao Tung University, the Taiwan Semiconductor Industry Association; the National Science Council; and the Bureau of Industry, Ministry of Economic Affairs. In *Korea*, this includes institutions like the relevant policy planning divisions of the Ministry of Information and Communication (MIC) and of the Electronics and Telecommunications Research Institute (ETRI). In Kuala Lumpur, I am to Dato Prof. Dr. Zawai Ismail, director, Commerce Asset Ventures, who has set up brainstorming sessions with relevant government agencies and venture capital firms. In Penang, I am indebted to discussions with Tan Sri Dr. Koh Tsu Koon, Chief Minister of Penang, Dato Dr. Toh Kin Woon, Penang State Executive Councillor, Mr. Boonler Somchit, Executive Director of the Penang Skills Development Centre (PSDC), Dr.Ganesh Rasagam, CEO, DCT Consultancy Services, and Dr. Anna Ong, Senior Analyst, Socio-Economic and Environmental Research Institute (SERI).

[12] Ray Bingham, president and CEO of Cadence Design Systems Inc, one of the leading vendors of electronic design automation (EDA) tools, quoted in Electronic Engineering Times, 28 February 2003

resistors) and their interconnecting 'wires' on a printed circuit board (PCB)[13] (Ernst and O'Connor, 1992, chapter IV). Note that, while design complexity is low for a simple single-layer board, it rises substantially for very complex multi-layer boards (some up to 18 or 24 layers, for notebooks). Combined with the experience in detailed product design and engineering that Asian firms have accumulated in the fabrication of high-precision components (like ICs), board-level design has given rise to a broad portfolio of design implementation capabilities. This explains why today Asian original-design manufacturers (ODMs) like HonHai, Mitac, Delta and Acer from Taiwan, NamTai from Hong Kong, and dozens of other Asian companies are able to compete successfully with the leading US-controlled global electronic manufacturing services (EMS) providers, like Flextronics or Solectron (Ernst, 2003a).

A third carrier of Asian design capabilities are fabless chip design start-up companies, especially from Taiwan like Etron, Via, or MediaTek. When these companies first entered the market, during the late 1980s, they were focused on semi-custom or ASIC design, where the goal was to avoid the very high cost and time required to design a full-custom IC[14]. An important catalyst was the establishment of Taiwan Semiconductor Manufacturing Corporation (TSMC) in 1987 as a provider of contract chip fabrication ("silicon foundry") services for "chipless" design companies. This enabled Taiwanese chip design start-ups to gain privileged access to a low-cost, high-speed supporting manufacturing system that encompasses both assembly and test, and wafer fabrication.

An equally important enabling factor for the entry of Asian chip design houses was the emergence of global EDA (="electronic design automation") tool vendors (like Synopsys, Cadence and Mentor). ASIC design required well-defined procedures to develop and use cell libraries that contain design modules. To do this cost-effectively, a new design methodology was developed where the design requirements were implemented in a software language that described digital circuits at the so-called register-transfer level (RTL) (see again **Figure 1**). To implement this new design, access to increasingly sophisticated EDA tools was critical. As these tools were available on the market, albeit at a very high price, this provided entry opportunities for Asian design companies. And as the effective use of these tools always require substantial tweaking and adjustments, these Asian companies were able to accumulate a broad set of capabilities related to the implementation of these increasingly automated design methodologies.

Relying on foundries and EDA tools enabled Asian, and especially Taiwanese design companies to concentrate their limited resources on pursuing a consistent niche strategy. The focus has been on design implementation and on organizational innovations that make it possible to reap as much benefits as possible from competitive strengths in speed, cost, flexibility and quality (Chang and Tsai, 2002). This has resulted in a rapid growth of Taiwan's fabless chip design industry, producing a 31% compound annual growth rate between 1995 and 2001[15]. In March 2003, a survey conducted by *EETimes* identified 234 Taiwanese chip design companies (Nanda, 2003). Five of the top 20 worldwide fabless companies are from Taiwan; and two Taiwanese design houses have moved up to the number 5 and 6 spot, capturing 16% of total fabless revenues.

1.3. Upgrading of Design Capabilities

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[13] A printed circuit board (PCB) is an internally wired, typically rectangular, substrate which holds a number of electronic components. The internal wiring is accomplished through a series of photolitographic processes when the PCB is manufactured.

[14] An ASIC typically is composed of standard building blocks called "cells" that are designed to implement a specific customer application.

[15] During 2001, Taiwan's chip design industry's revenue growth was 18%, significantly outpacing the almost flat growth of the global chip design industry (ITRI, 2002)

All strategic groups in our interview sample have invested in chip design-related activities in Asia over the last few years, and/or are planning to expand such activities. While there are no systematic data on investment outlays and type of design activities, the interviews produced three general findings. First, global firms are expanding and upgrading their design centers in Asia as part of their GDNs. They consider the lower annual cost of employing a chip design engineer in Asia (between 10 and 20% of the cost in Silicon Valley (**figure 2)** to be an important pull factor. Additional pull factors include attractive tax rebates, a skilled and re-trainable workforce as well as easy access to foundry, assembly and testing services, and proximity to higher-end specialized network suppliers of components, manufacturing services and knowledge-intensive business services, especially design and engineering support services.

Figure 2: Annual Cost of Employing a Chip Design Engineer (US-$), 2002

Specific motivations differ across sectors and strategic groups. For mobile communication systems for instance, all major global system companies are expanding their Asian chip design centers to establish their own reference or "platform" designs[16] as *de facto* standards in the region. This reflects the growing importance of Asia as a major growth market for electronics products and services. As a result, global brand leaders in the electronics industry, like Intel, Microsoft, and Cisco, attempt to push their "platform leadership" strategies into Asia[17].

Second, leading Asian system companies (especially from "Greater China", Korea and India) are emerging as new sources of chip design, as part of their strategies to establish themselves as new sources of innovation and global standards. This includes innovations in process technology for electronic components (especially semiconductors and displays), where Korean and Taiwanese firms are among the industry leaders. But it also includes system specification (as defined in **figure 1**): Asian firms are now producing innovations in the design of complex system architectures[18] in sectors like digital consumer systems, wireless telecommunication systems, and business process software.

For instance, in consumer electronics, there are joint efforts by China and Taiwan to develop a new video-disk technology format, called EVD (enhanced versatile disk) that would allow resolution five times higher than the current de facto industry standard DVD, while helping China's consumer electronics industry to escape full royalty payments to the dominant DVD licensing groups. Beijing E-World Technology, a consortium of 10 Chinese DVD manufacturers, is conducting government-sponsored research, in collaboration with Taiwan's Industrial Technology Research Institute (ITRI), and Taiwanese disk makers and chip design houses.

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[16] The concept of "platform design" was first developed in the car industry, under the heading of "modular design" (Baldwin and Clark, 2000; Sanchez and Mahoney, 1996). To deal with increasingly demanding cost reduction pressures, car manufacturers used a common template architecture for different car models, allowing the sharing of molds and common elements, the "design modules". This design methodology was then applied to other industries, including the computer industry (Langlois and Roberston, 1992). In the semiconductor industry, "platform design" is an organised method to reduce the time required and risk involved in designing and verifying a complex system-on-a-chip (SoC), by heavily and systematically reusing as many design steps as possible (Chang, 2003:23).

[17] "Platform leadership" strategies are defined by decisions on the "system architecture (the degree of modularity), interfaces (the degree of openness of the interfaces to the platform), and intellectual property (how much information about the platform and its interfaces to disclose to outside firms)" (Gawer and Cusumano, 2002: 40).

[18] Computer designers use the term "architecture" to refer to "the partitioning of the … (computer) … system into components of a given scope and related to each other functionally and physically through given interfaces. From a given architecture flows the design of components' functions and how they relate to each other…" (Gawer and Cusumano, 2002: 18). These authors compare a system architecture with a geographic map, where the components of the system are the countries' territories and the interfaces between components are the countries' borders (ibid.:19).

In telecommunications, Korea's four leading players (Samsung, SK Telecom, KT, and LG) are all engaged in serious efforts to become major platform and contents developers for complex technology systems, especially in mobile communications. These efforts can build on considerable capabilities, accumulated in public research labs (like the Electronics and Telecommunications Research Institute, ETRI), as well as in R&D labs of the chaebol, to develop complex technology systems like TDX (a switching system) and communication systems that are based on the CDMA (= code-division multiple access) standard.

Furthermore, China's attempt to develop an alternative third generation (3G) digital wireless standard, called TD-SCDMA (time-division synchronous code-division multiple access), has created a powerful motivation to expand Asian electronic design activities for all strategic groups in our interview sample. The TD-SCDMA standard was developed by Datang Telecom, a Chinese state-owned enterprise, and the Research Institute of the Ministry of Information Industry, with technical assistance from Siemens[19]. To accelerate the implementation of this strategy, Datang has formed a series of collaborative agreements: a joint venture with Nokia, Texas Instruments, the Korean LG group, and Taiwanese ODM (= original design manufacturing) suppliers; a joint venture with Philips and Samsung; and a licensing agreement with STMicroelectronics that will provide the Chinese company with access to critical design building blocks.

And third, as chip and system design are expanding in Asia, this creates significant new entry possibilities for Asian specialized suppliers of a broad array of design implementation services. As we will see below, this reflects the combined impact of radical changes in design methodology and organization, and of the huge implementation problems involved in transferring these methodologies and organizational structures to distant locations. As the six non-shaded boxes in the middle of **figure 1** demonstrate, there are multiple possibilities for segmenting the market for design implementation services, providing ample opportunities for niche market entry strategies for mid-sized companies.

In short, there is reason to believe that the development of Asian chip design capabilities has passed a critical minimum threshold. Of course, global R&D remains highly concentrated - 85% takes place in only seven industrialized countries, with the U.S. occupying the leading position with 37% (Dahlman and Aubert, 2001, p.34). For instance, China's total R&D spending is about $ 11billion, compared to more than $233 billion for the US. And the R&D budget of a U.S. industry leader, Microsoft, at around $ 6.2 billion (for 2003), exceeds 56% of China's total R&D budget. Nevertheless, there are clear signs that Asia's leading electronics exporting countries are entering the "global innovation race" (Baumol, 2002). In a handful of emerging centers of excellence in Asia, sophisticated innovation and research capabilities appear to have followed the earlier development of electronics manufacturing capabilities. This is likely to add further to the development of Asia's chip design capabilities. Let us now turn to possible explanations that result from current changes in design methodology and organization, and from the spread of global design networks (GDNs).

2. System-on-Chip (SoC): Upheaval in Design Methodology

Over the last few years, intensifying pressures to improve design productivity, combined with increasingly demanding performance requirements for electronic systems have produced an upheaval in both design methodology and organization. Under the label of "system-on-chip" (SoC) design, radical changes in the methodology of design attempt to combine "system-level integration" on a chip with "modular design" and "design automation". This is expected to

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[19] Approval by the International Telecommunications Union (ITU) was granted in August 2000. The two dominant competing global 3G standards are W-CDMA (compatible with existing GSM operations, and supported by European firms), and CDMA 2000 (compatible with existing CDMA operations, and supported by US firms).

facilitate the reuse of design building blocks, the so-called "silicon intellectual properties" (SIPs). In turn, these new methodologies require drastic changes in organization. There are attempts to transform an erstwhile loosely organized *artisan-type* activity into a highly routinized *factory-type* operation where most design stages can be automated.

I first review the new challenges for chip design that result from a widening productivity gap between design and fabrication, and from increasingly demanding performance requirements. I then examine changes in design methodology and tools that are emerging in response to the above two challenges. Throughout this analysis, I will highlight how changes in design methodology have increased both cognitive and organizational complexity, pushing for geographic dispersion.

2.1.New Challenges

A widening *productivity gap* between design and fabrication has been a primary driver behind changes in design methodology and organization. While the productivity of semiconductor fabrication over the last twenty years has seen a 58% compounded annual growth, the productivity of chip design has lagged behind, with only a 21% compounded annual rate (**Figure 3**). According to the International Technology Roadmap for Semiconductors 2001, the bible of the semiconductor industry, the spiraling cost of design is the greatest threat to a continuous growth of this industry (ITRS, 2002: 81). Design costs massively outpace the cost of chip manufacturing. Manufacturing costs for chips, the so-called non-recurring engineering costs (NREs) that cover masks and probe card, are exceeding $ 1 million. However design-related NREs routinely reach tens of millions of dollars, with design shortfalls being responsible for massive corrections in fabrication that multiply manufacturing NRE.

Figure 3: Widening Design Productivity Gap in Integrated Circuits

There is also an important time dimension to this gap. Time-to-market is of critical importance in the semiconductor industry, as rapid technology change shortens product-life-cycles. Again there is a growing imbalance between manufacturing and design. Manufacturing cycle times are measured in weeks, with low uncertainty. However, design and verification cycle times are measured in months or years, with high uncertainty. In the end, the *design productivity gap* reflects a growing gap between process and design technology. Over the last years, the number of available transistors has grown faster than the ability to design them meaningfully (ITRS 2002: 81). Miniaturization has resulted in chips of sub-micron feature size - it is now possible to fabricate millions of transistors on a single chip. The challenge for chip design thus "…lies not in making the densest of chip but in filling up the vast area of silicon that is now offered."[20] The resultant increase in design complexity must be matched by an equally dramatic improvement in design implementation productivity (ITRS 2004: 13,14).

However, investment in process technology has by far outpaced investment in design technology. And, most disturbingly, the cost of design keeps growing exponentially, reflecting increasingly complex design requirements (**Figure 4**). For instance, $ 22 million are required to implement a 20 million gate design at the 90 nanometer (nm) process technology (IBS 2002: 67). This estimate covers "only" the cost for designing the hardware, from generating the specifications to delivering the validated prototype. To this needs to be added the increasing share of software costs. At the 90 nm level, the software design costs are substantially higher than hardware design costs, i.e. $ 30 million out of a total of $ 52 million[21]. As global silicon

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[20] Email to the author by Prof. Ismail Zawawi, Kuala Lumpur, Malaysia, October 3, 2002.
[21] Other estimates, presented at the 2003 International Symposium on the Quality of Electronic Design (ISQED) point an even bleaker picture of SOC design costs spiraling out of control to reach $ 80 million for an "ambitious"

vendors (both IDMs and fabless design houses) typically have insufficient software design capabilities (IBS 2002: 57), this indicates a huge potential for outsourcing to emerging lower-cost software clusters in Asia.

Figure 4: Costs of Implementing New Designs

An equally demanding challenge for chip design are the increasingly demanding *performance requirements* for electronic systems. This has substantially raised both the cognitive and the organizational dimensions of design complexity, very much in line with Pavitt's conceptualization. The key to success in chip design is a capacity to do two things simultaneously: to be first in using leading-edge process technology to produce the lowest-cost device, and to design differentiated performance features that meet real needs. To find out what are real needs requires permanent and very intense interaction with customers, end-users and other relevant market participants. Identifying user needs has become more challenging. One reason is that the PC sector has lost its erstwhile dominant position as the main driver of chip demand, producing more segmented and differentiated demand patterns. A second important reason is that major growth markets, as well as test-bed and launch markets are no longer restricted to the US, Western Europe and Japan, but include now markets in Singapore, Korea, India, and especially Greater China.

The convergence of digital computing, communication and consumer devices has produced a variety of electronic systems that all strive to become lighter, thinner, shorter, smaller, faster and cheaper, as well as more multi-functional and less power-consuming. Time compression is essential in designing chips for such systems. As product life cycles for electronic systems become shorter and shorter, in many cases as short as a few months, chip design cycles of months or years are no longer acceptable. Performance requirements appear to be most demanding for portable, wireless, broadband, Internet switching, mass storage, and computers server systems. For instance, for portable and wireless systems, there is tremendous pressure to improve both size/weight ratios and battery life (ITRS, 2002: 61). Essential performance features are expected to double every two years, time-to-market is critical, and product-life-cycles are rapidly shrinking to a few months.

As a result of these demanding performance requirements, chip design teams must cope with complex trade-offs that can easily spiral out of control into multiple vicious circles. For instance, optimization for clock speed needs to be combined with optimization for area, power consumption and production cost, while it is necessary to reduce overall design time and cost. Ensuring that a chip will run at the desired speed becomes substantially more difficult as transistor sizes move to 130 nanometer and below. In addition, with growing design complexity, design cycle time grows, and it becomes increasingly difficult for designers to incorporate the growing number of changes in design specifications that are typical for emerging and fast-moving markets for chip applications, like mobile phones or digital consumer devices. To cope with this challenge would require a capacity for rapid adjustments in design. This however poses a strategic dilemma: How to balance trade-offs between design flexibility (which typically involves extra cost) and attempts to improve productivity?

2.2.Changes in Design Methodology

"Design methodology" is the sequence of steps by which a design process will reliably produce a design "as close as possible" to the design target, while maintaining feasibility with

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90nm SOC design, requiring 4 million lines of HDL code and a core team of at least 50 engineers ("ISQED speakers propose profound changes in chip design", 2003).

respect to constraints. All known design methodologies combine (1) the enforcement of system specification and constraints via top-down planning and search, with (2) a bottom-up propagation of constraints that stem from physical laws, limits of design and manufacturing technology, and system cost limits. Traditional design methodologies are no longer able to cope with the challenges that I have described before. Under the label of "SoC" design, there are now systematic attempts under way to enhance design methodology through a combination of "system-level integration" on a chip, "modular design" and "design automation".

In contrast to initial expectations, both cognitive and organizational complexity significantly increased as a result of attempts to move design from the individual component on a printed circuit board closer to system integration. As we will see in part 3, this growing complexity has created powerful pressures for vertical specialization: design teams had to be extended beyond the boundaries of the firm; they also had to be geographically dispersed across national borders.

Attempts to increase the system level of chip design originated in Sematech, the U.S. consortium established to reinvigorate the American semiconductor industry. An important document that laid out in some detail key features of the SoC design concept has been the National Technology Roadmap for Semiconductors, published by Sematech in August 1994. Reflecting the pervasive globalization of this industry, this debate has rapidly proliferated internationally. Since 1998, this document has become the International Roadmap for Semiconductors (IRTS), which is now jointly published by the US. Semiconductor Industry Association, as well as by the by the relevant industry association of the European Union, Japan, Korea and Taiwan.

As befits such a drastic change in design methodology, initial expectations were very high. An influential study by the director of engineering of Synopsys, a leading EDA tool vendor, claimed that systematic and effective design reuse would reduce chip-development costs by 50% in three years and by more than 70% in six years, compared with the cost of developing chips without reuse (Keating, 1998)[22]. In addition, an abundance of surplus venture capital during the "New Economy" bubble created a euphoric "race to higher integration"[23]. However, the initial euphoria was soon followed by disappointment. Since 1999, the annual number of chip design starts remained flat. To some degree, the stagnation in the number of new design starts reflects of course the move to SoC design: a shift to higher levels of system integration allows the contents of several ICs to be combined into one integrated SoC or into a more highly integrated system-in-package (SiP). But the slow-down in the growth of the chip design market was primarily due to a combination of two developments, one cyclical and one structural. The downturn in the global IT sector had a devastating impact: "…(F)uelled by the bursting of the "dot.com" bubble, the collapse of the grossly overvalued communications sector, and a fair degree of corporate and Wall Street shenanigans, …(the electronics downturn)… has brought gloom, layoffs, and collapse to a large part of the industry. IC design has been no exception." (Martin, 2003: 9)

An equally important structural cause was what industry insiders call the "SoC crisis". It soon became clear that, while a shift to system-level design based on modularization is overdue, its implementation is going to be very, very difficult (e.g., Roberts, 2001; Claasen, 2003). To quote two chip designers of India's WIPRO Technologies: " while the potential is huge, the complexities are several, and countering these to offer successful designs is a true engineering

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[22] This however would require that by 2000 at least 50% of all chip design projects would rely on design reuse. The Synposys study emphasized that, without reuse of design modules, the cost of chip design would explode from $ 3million per chip to $193 million.

[23] "No matter how much your design capital requirements were, if you had the right buzzwords in your business plan - heck, if you even had a business plan - you were encouraged to take more. So no one balked at pulling together a design team twice the size that anyone in the management had ever managed before" ("Low integration can up returns", 2002).

challenge" (Kamath and Kaundin, 2001). What initially looked like a panacea, turned out to have produced quite mixed results. This is in line with Rosenberg's well documented insight that the real impact of important innovations is seldom realized immediately, but requires countless iterations and re-combinations with other complementary innovations (e.g., Rosenberg, 1976: ch. 11).

This crisis in SoC design has worked as a powerful catalyst for attempts to reconsider existing strategies to reduce the design productivity gap. There is a growing recognition in the design community that, as long as the new design methodology is not well established, and as long as skills and design tools lag well behind increasingly complex design and verification requirements, SoC designers will face rising costs and entry barriers. In line with Pavitt's conceptualization of cognitive complexity, verification and testing have become a critical bottleneck (Pavitt, 1999: p.X). With growing design complexity, it becomes necessary to verify early and frequently whether the SoC design can be produced at sufficiently high yield, and whether it will do what it is expected to do. Today, 60 to 70% of SoC hardware design time goes into verification, leaving only 30 to 40% for the actual device development. This obviously constrains considerably the productivity of design. Attempts to cope with this "verification crisis" emphasize the modularization of verification programs, to enhance the reuse of successful modules ("Solutions proposed for verification crisis", 2002). In turn, this increases the pressure for vertical specialization.

Overall, the emphasis of the debate has shifted from the benefits to the limits to system integration. According to a vice president for design at Motorola, " a single-chip GSM handset would require three to four years, a 300-person design team and would be sadly uncompetitive." (Ken Hansen, quoted in "SoC slam dunk still slightly out of reach", 2003). This implies that system integration may work for some applications, but not for others. For each device, it is necessary to find the right balance along a continuum between the traditional board-level design and a single large and extremely complex SoC. In addition, "…(n)ot only has the assumption that higher integration is mandatory been undermined, but the means to achieve it have been dissolved as well…If you are not self-funded then you'd better have at least one customer ready to make the rounds in Menlo Park with you." ("Low integration can up returns", 2002).

After the bursting of the "New Economy" bubble, it has become very difficult and costly for design houses to win design-ins from global set makers. This reflects the extremely cautious approach of set-makers to new product development. For chip design, this implies that improving performance features (the main concern of set-makers) needs to be combined with a relatively conservative approach to design that helps to avoid low manufacturing yields[24]. However, our interviews show that Asian system companies are more willing to use new and unconventional chip designs. Their main concern is whether these designs will enable them to reach their main objectives, i.e. to improve both speed-to-market and market penetration. This sets the Asian system companies apart from the global market leaders who are more cautious and unwilling to shoulder the higher costs and risks of innovative designs. As this signals a shift in the market for SoC designs to Asia, this may provide a further powerful incentive for global IDMs and design houses to relocate chip design to that region.

2.3. Response: "Platform design"
There is a growing consensus that, to turn the tide and to improve the benefits of system-level design, drastic improvements are required in design methodologies. All major actors in the semiconductor industry are now engaged in a process of searching for more effective design

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[24] This pressure to focus design on acceptable fabrication yields increases as yields tend to fall quite drastically with progressive process miniaturization (Edwards, 2003: 7)

implementation strategies. One important approach are attempts to push chip design even closer to the system level, through "platform design" (Martin, 2003: 12-15; Chang, 2003, pp. 24 ff). Each SoC design requires all the steps shown in **figure 5**. However, by performing many of the steps only once across many similar SoC designs, platform design is expected to reduce the time required and risk involved in designing and verifying a complex SoC. Platforms design attempts to capture and reuse the "best architectures and design approaches found for particular types of products and markets… (Platforms) "crystallize and harden these approaches for reuse by others." (Martin, 2003: 13).

Figure 5: Overview of Steps in an SoC Design

The overall result is a substantial increase in design complexity, which in turn fosters vertical specialization pressures. The move to platform-design thus is likely to enhance the spatial mobility of chip design. Once a library of "best architectures and design approaches" exists for multiple design steps required for an SoC design, this can facilitate the exchange of knowledge "from more experienced design teams and architects to less experienced designers." (Martin, 2003: 13). Platform design thus facilitates the disintegration and geographic dispersion of design teams to multiple locations with different, yet complementary specialization profiles. Our interviews confirm that the shift to platform design may be accelerating the relocation of chip design to Asia.

Platform design is shaped by the performance requirements of the electronic systems as well as the constraints imposed by the SoC design methodology and the design rules of foundry service providers. In addition, standards play an increasingly important role in dictating platform design. This has given rise to attempts by a growing number of global brand leaders in the electronics industry, like Intel, Microsoft, and Cisco, to develop "platform leadership" strategies[25]. These strategies have two objectives: to avoid the very high costs and risks of trying to develop complex technology systems in-house; and to enhance and control patterns of innovation in an industry. The over-riding purpose of these strategies is to leverage the existing market power of industry leaders (the "global network flagships" in our terminology) into the control of "systemic architectural innovations" (Gawer and Cusumano, 2002: 39). A typical example are Intel's attempts to extend its control over microprocessors by creating widely accepted architectural designs that increase the processing requirements of electronic systems, and hence the market for Intel's microprocessors.

It is important however to emphasize that these strategies critically depend on vertical specialization, and that this may provide new entry possibilities for small network suppliers. To implement "platform leadership" strategies, a flagship like Intel needs to stimulate external innovations by independent specialized suppliers for a variety of components of this new system architecture. As long as "modular design" provides "open" interfaces between system components, Intel believes that "many more innovations could emerge from a computer industry organized in layers of specialized firms" (Gawer and Cusumano, 2002: 45) that design such hardware and software components. These platform-centered innovation networks initially were centered on the US. But, as we saw in part 1 of this paper, platform leaders like Intel are now rapidly expanding their chip design centers in Asia.

An important impact of the move towards "platform design" is to increase vertical specialization at each step of chip design. Take "embedded software (ESW) design" which on average now requires two to three times the effort compared to hardware design. Software design

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[25] See note 17.

is rapidly increasing in importance. According to the executive vice president of technology and strategy at Philips Semiconductors, software is about to become the "next bottleneck" in SoC design: "the amount of software - for applications like multimedia cell phones, PDAs, and digital televisions - is increasing exponentially, while the efficiency of software design is not keeping pace." (Claasen, 2003: 24) As we have seen before (**Figure 4**), this has produced a massive increase in the share of software design costs. If correct, these projections imply that pretty soon SoC design will become software design. This may well further facilitate the vertical specialization within chip design, as well as the geographic dispersion of design capabilities to the sprawling software engineering clusters in Asia, primarily in India and Greater China.

An important characteristic of ESW design is that it is much more demanding than developing application software for PCs (Chang, 2003: 28). As every PC user knows all too well, reliability and ease of use has not been a major concern for PC software. This is very different for ESW design. In addition to very tight cost constraints, user demands for reliability and ease of use are critical for devices like mobile phones or digital AV equipment. An important challenge is to overcome daunting legacy problems, to ensure portability, which is much more difficult to achieve for embedded products. This requires tedious work by highly skilled software engineers. These characteristics make ESW design a strong candidate for relocation to Asian software clusters.

Finally, important changes are under way in the concept of "design platforms". These changes reflect the rapid pace of change in the chip design industry, and they may create new entry possibilities for chip design in Asia. The traditional taxonomy of "design platforms", reported in Linden and Somaya (2003: 18), distinguishes hard, firm and soft SIPs. Hard SIPs are provided as mask-level data that is adapted to the process technology of a particular foundry, and hence permits the fastest implementation. Soft SIPs however provide a more abstract description of architecture and algorithm with no physical layout, and hence provide much greater flexibility for adaptation to a specific application, enhancing the scope for product differentiation. But that advantage comes at a substantial cost, especially for smaller players: it takes much longer to implement soft SIPs, and licensing fees are much higher.

A new taxonomy is emerging of vertical specialization through platform design distinguishes three configurations. "Full application platforms" provide a complete implementation vehicle for specific product domains, like for digital video applications (e.g., Philips) or for wireless devices (e.g., Texas Instruments). Such "full application platforms" are attractive for Asian set makers who focus on rapid and aggressive market penetration. However, the development of such platforms is extremely costly and risky, leaving this as an option only for leading global players, like Samsung or, possibly China's Haier and TCL. Platforms can also be "processor-centric", where specialized global SIP suppliers like ARM, concentrate on the processor, its required bus architecture and basic sets of peripherals. Being more generic than the full application platform, they take less effort to develop, and they pose a lower investment risk for the SIP suppliers. But more work is required by the design house to turn such "processor-centric" platform into a SIP that can be effectively used in a specific SoC design. Finally, "reconfigurable platforms" (provided by global specialized suppliers like Xilinx and Altera) deliver core processors plus so-called re-configurable logic along with associated SIP libraries and design tool flows (e.g., Lysaght,2003; Kempa et al, 2003).

3. Changes in Design Organization

In the search for solutions to the "SoC crisis", most of the technical literature has focused on changes in design methodology and tools. However, there is a growing consensus that, for the new methodologies and tools to produce the expected results, fundamental changes are required

in the organization of design as well as in the institutional environment. But the most fundamental requirement is access to human resources. SoC design drastically changes the nature of design work: design is not just done faster, it is done differently by different people, and the relationship between designer and design is fundamentally altered by introducing vertical specialization. SoC design teams need to be able to recruit and retain highly experienced design engineers who master a portfolio of critical skills and capabilities. Such design talent is scarce everywhere, and hence SoC design teams need to recruit and retain them wherever they exist, and this is increasingly in Asia.

I first highlight the quite drastic changes in design skill requirements, brought about by the transition to SoC design, and the transformation of design work organization into a factory-type operation. I will then examine attempts to reduce the so-called behavioral and cultural barriers (or in plain words: resistance) to these transformations, focusing specifically on the reuse of chip design knowledge. I argue that both changes in design organization are creating pressures to relocate design to new, lower-cost locations in Asia.

3.1. Skill Requirements and Work Organization

A widely quoted study prepared for the *Electronic Design Automation Consortium*, highlights the "limited number of engineers available worldwide to implement complex designs" as a critical challenge for a successful transition to SoC design (IBS 2002: 13). One possible explanation may be a serious mismatch between the supply of skills in the existing designer population and the quite different skills required by the transition from board-level to system-level chip design[26]. An equally important explanation may be a growing mismatch between what designers expect to earn and what design firms are willing and able to pay. During the "New Economy" boom of the 1990s, U.S. designers were used to receive generous stock options and other incentives. Since the downturn however, practically all strategic groups in our interview sample with non-Asian ownership have been exposed to intense cost-cutting pressures. In addition, SoC design requires a highly routinized, almost factory-type organization of design work, which is very much in contrast to the expectations and self-perceptions of IC designers in the US and Europe. For them what counts in their resumes is to have "authored" original "breakthrough designs" which, as we will see below, is very different from the daily routine of SoC design.

Skill requirements for SoC design share common features with ASIC design. A majority of the designer population however are board-level designers. The skills they have honed over the years in systems board design are very different from the new skill set required for SoC design. Some board-level designers may find niches to survive in design teams of global set makers. But most board-level designers will have to go through a difficult process of unlearning and re-learning. For instance, quality requirements are much more demanding: with SoC mask sets costing up to $ 1 million, design quality must adhere to "right first time" methodologies. While a board designer must be good in tweaking design prototypes, this is no longer possible with SoC design. Instead of tinkering, based on accumulated design experience, much more abstract thinking is required. A particularly demanding change in skill requirements is that SoC designers need to be much more open and knowledgeable about the use of software. At the same time, SoC designers need to be prepared to constantly learn and unlearn, as design methodologies are still in flux. This requires a willingness to adjust to abrupt changes in design procedures.

In response to these changes in design skill requirements, a thriving market has emerged for design training and re-skilling services. The providers of such services include specialized

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[26] Unfortunately, while everybody in the industry talks about this so-called "designer bottleneck", very little research has been done on possible causes.

private training organizations and public research institutes[27]. In fact, progressive vertical specialization within chip design can only produce expected results, if it is accompanied by a parallel process of re-integration and coordination through diverse public-private cooperation schemes that foster collaboration between university labs, industry and government agencies. Asia's leading electronics exporting countries have been quick to develop their own set of private and public SoC design training institutions that could foster the development of new specialized chip and system design clusters (Ernst, 2004a; Ernst forthcoming a).

The increasing complexity of SoC design requires massive changes in the organization of design work: an erstwhile loosely organized artisan-type activity needs to be transformed into a highly routinized almost *factory-type* operation. Board-level designers are used to work in small teams and to see a whole design through to completion. Yet, SoC designs tend to be done in very large teams, spread across different countries and time zones. The typical team size for an SOC design can range from 50 to 60 engineers (up from around 10 for board-level design), each designer with annual loaded cost of $250 K to $350K. And to complete an Intel processor design can take two years and involves thousands of people in different countries, which requires a highly structured and disciplined factory-type work process[28]. This is so, because with growing team size and with geographic dispersion of design teams, coordination costs rise, comprising now around 20 to 30% of the total design implementation costs (IBS 2002: 67).

To cope efficiently with these demanding coordination challenges requires design team managers with holistic "bridging capabilities" (author's interview in major Taiwanese foundry, September 22, 2003) between the various disciplines involved in the different teams of an SoC design network. As this requires a robust understanding of the myriad operations involved in SoC design, these people are very difficult to find. In addition, there is a growing need for design "operations analysts". Yet, in contrast to chip fabrication, there is limited progress in operations analysis for chip design. While there is a broad consensus that silicon-proven SIPs are critical, there has been little progress in operationalizing this concept. Benchmarking techniques for design performance are crude and under-developed[29].

In addition, chip designers love to produce complex breakthrough designs, by pushing the envelope of design methodologies. These ambitions are frustrated by the move towards more structured and conservative design approaches that emphasize incremental progress through the reuse of existing SIPs. Many designers complain that this "just doesn't look great on a resume." (author's interviews with Taiwanese design company, September 2003).

Most important however are changes in design procedures that reflect the tremendous pressures to improve design productivity. SoC designers must incessantly strive to cut cost and time-to-market for increasingly complex devices, which gives rise to an intense workload. "Bleeding-edge designers today confront 20 million-gate, six-level-metal design, in projects that may be divided among teams of 40 or 50 engineers. It's not a job for the faint of heart."("SoC designers describe their 'best practices'", p.1). It is typical that SoC designers "work six days per

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[27] Private SOC design training firms are mushrooming in all major electronics industry clusters. As for public training institutions, the role model is Scotland's Institute for System Level Integration (ISLI), based on the Alba campus outside of Livingston, which was formed specifically to train people for SOC design. The EC is offering advanced SOC design courses through SYDIC, a program under the auspices of ECSI, the European Electronic Chips and System Design Initiative. SYDIC coordinates the resources of organizations such as ISLI, IMEC , and also involves major EDA tool vendors. More recently, a group academics, assisted by industry is seeking EC funds to create a Europe-wide network of excellence for SOC development and engineering courses The initiative, named EuroSOC, brings together 210 SOC communities from 160 institutes, each with its own industry.
[28] Rudy Lauwereins, vice president of design technology at the Belgian microelectronics research institute IMEC, as quoted in Collins (2003:9)
[29] "In general, IC vendors either do not benchmark their design capabilities very thoroughly or the benchmarking efforts do not realistically assess their capabilities" (IBS, 2002: 56)

week, twelve hours per day, with intense pressures to meet the time-to-market requirements for design" (IBS 2003: 42). Obviously a 72 hours work week will come at the cost of innovation, even if incentives through stock options are high. But as pressure grows in the U.S. to expense stock options, it is difficult to see why designers there would be willing to keep up with such health-destroying work loads. That may be different however in Taiwan and China, where the system of personal income taxation enables semiconductor personnel to receive company stock and options as compensation in a manner which results in little or no actual income or capital gains tax being paid when the stock is sold. As a result, Taiwanese and Chinese firms arguably "…have a competitive advantage (the lure of rapid personal accrual of substantial wealth) with respect to competition for talent that other firms cannot match." (Howell et al, 2003: IV)[30]

3.2. Barriers to the Reuse of Design Knowledge

A leading textbook on SoC design compares it with Henry Ford's assembly line, with engineers putting systems (i.e., cars) together out of parts previously designed in another group, in another country, in another company (Chang et al, 1999, p.17). If this view were correct, this would indicate that the organization of chip design work somewhat belatedly follows a path trodden earlier by hardware manufacturing.

However, a comparison with Fordism may be misleading. Engineers like to talk about "virtual components", when they describe the design building blocks (the SIPs) that need to be exchanged between various participants in the interactive design process. But the real challenge posed by the transition to SoC design is to develop an organizational set-up that facilitates the exchange and reuse of design knowledge. Much of this knowledge exchange involves tacit knowledge, hence work organization needs to differ from traditional Fordism. Brute force cannot cope with the high transaction costs involved in exchanging very complex design knowledge. And rigid Fordist organizational principles would carry a high risk of obstructing speed-to-market due to opportunistic behavior. While Fordist work organization focuses almost exclusively on cost reduction through scale economies, the reorganization of SoC design is expected to cope with increasing complexity, and to improve design productivity. It is thus hardly surprising that attempts to impose a Fordist work organization have made little progress. Where changes occurred, like in ASIC design cell libraries and in software object libraries, Fordism has been tampered with elements of flexible production.

There is no doubt that cultural and behavioral barriers to the reuse of chip design knowledge are the most important constraints to the implementation of SoC design. To understand why, we need to address the puzzling question why proximity can be advantageous, but also disadvantageous for the reuse of complex design knowledge.

Apparently, the reuse of design knowledge is spatially sticky: knowledge reuse works well, as long as this knowledge is embedded in individual designers, or small specialized design teams. One way to do this is to place everyone literally in one room. The so-called "boiler room" model, where dense informal contacts between designers result from having coffee and lunch together, is unbeatable when the objective is to exchange complex tacit knowledge (Wilson, 2003: 49). A second approach is the so-called "journey men" model, where successful design teams tend to stay together, moving as a group from one company to another, or to new locations. Sometimes, these design teams even tend to maintain the same SIP vendors from job to job, "preserving interfaces that have evolved through trial and trouble and that have come to be trusted." (Wilson, 2003: 62).

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[30] In Taiwan and China, employees of semiconductor firms who have received stock as compensation are taxed on the face value of the shares, not the market value - which is often many times higher than the face value, given the rapid growth of semiconductor firms in both countries.

In both case, what is reused is the knowledge in the team members' heads, as well as their experience with the processes, tools, and technology they used. But once another engineer or another engineering team is asked to reproduce this design, little productivity increase is observed. This shows that, in principle, the arguments for proximity and co-location of design remain as powerful as ever. The challenge for innovation theory is to explain why sometimes proximity also poses substantial disadvantages.

One possible explanation may be that cultural and behavioral barriers to the reuse of design knowledge are deeply entrenched in particular localities. For instance, chip design engineers in the US have a tendency to invent wherever possible, rather than to simply reuse existing design modules (SIPs). This so-called "not invented here" syndrome is difficult to change, as it reflects the pride of an engineer who has found a more elegant design solution. Other such barriers include an unwillingness to accept a heavily constrained environment (a "design factory"), or an inability to create an acceptably constrained environment (Chang et al, 1999, p.18). In our interviews, global firms indicated that attempts to bypass persistent behavioral barriers to SoC design have played an important role for the relocation of design stages to Asia.

3.3. Reuse of Design Knowledge - Alternative Models

To overcome these barriers requires fundamental changes in organization as well as in geographic location. Reuse of knowledge can only work if adequate documentation exists, and if there are robust standards and procedures for knowledge exchange that prevent opportunistic misuse of shared knowledge. This necessitates a transition from personalized to more structured and formalized models of knowledge exchange. Without such organizational adjustments, designers are right to argue that learning and adapting what has been done elsewhere takes longer than starting from the original specification.

To highlight this important issue, let us distinguish four alternative models of reuse of design knowledge: personal, source, core, and virtual components[31]. In the *personal* reuse of design knowledge, that knowledge is embedded in individual designers or in small, homogeneous and largely self-contained design teams. Apart from the "not invented here" syndrome, two problems obstruct the effectiveness of knowledge exchange. First, it is difficult to retain key personnel, as top designers want to work on the next system rather than on what they perceive to be "derivates". Second, there is also a danger that individual designers get too much attached to a particular technology, architecture or design methodology. Once the design house is forced to change any or all of these three features, this may significantly undermine design productivity.

A limited reuse of general-purpose, unverified *source* files helps to address some of the weaknesses of the *personal* reuse of knowledge. However, it also carries many imponderables. For instance, this approach will only work, if the original designer is available to answer questions, a heroic assumption in an industry characterized by high job mobility, and, more recently, massive retrenchments. This second model of knowledge reuse also requires an openness of the adopting designer to use an existing design, rather than coming up with her own, presumably much more elegant solution. Further, the *source* model of knowledge reuse is normally hampered by insufficient documentation, with the result that the time to evaluate and understand what is available often takes longer than to produce an original design.

The reuse of application-proven *cores* with a physical and project history attempts to overcome the last constraint. An improved database enhances documentation, and hence the scope for knowledge reuse. Reusable design building blocks can be drawn from a clearly specified design library. It now becomes possible to form multi-group, multi-disciplinary design groups, consisting of system designers, chip integrators, and so-called "block authors", who

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[31] I draw on Chang et al, 1999, pages 18-25; ITRS 2002 and 2004

create specific design blocks (SIPs). However, physical proximity is still an over-riding concern, as many iterative adjustments are required.

The transition to *virtual components* brings us to a much higher degree of design modularization. "Virtual components" are design blocks that are available in the market, that are ready for reuse, and that have been successfully manufactured and used in relevant applications. In the parlance of design engineers, virtual components are "pre-characterized, pre-verified, and pre-modeled blocks….designed to target a specific virtual system environment" (Chang et al, 1999, p. 24). Like hardware components, these virtual components can easily be exchanged, as they have been created and tested according to very demanding standards. It is expected that, by outsourcing virtual components, it will be possible to sustain a clear-cut separation between the creation ("authoring") of a particular design block and the task of design implementation.

In other words, knowledge reuse through "virtual components" is expected to reduce constraints to geographic dispersion, which would help to reduce resistance to emerging factory-type forms of design organization. However, this would result in a highly unequal international division of labor, repeating earlier developments in the manufacturing sector, where cost-sensitive value chain stages have moved out to low-labor cost locations. Within this framework, the established global centers of chip design excellence would be able to retain the creative parts of design (SIP authoring and system specification). And only "blue-collar" chip design implementation tasks would move to Asia.

But, as we have seen in part 1 one the paper, this claim does no longer match with reality. To explain why, let us examine a new organizational model of chip design that I call global design networks (GDNs).

4. Vertical Specialization Within Global Design Networks

We have seen how radical changes in design methodology and organization have increased the cognitive and organizational complexity of chip design, creating a fertile ground for vertical specialization. Let us now turn to the final missing link of our argument: vertical specialization takes place within GDNs, and this in turn is facilitating the relocation of design to new, lower-cost locations in Asia.

This argument runs counter to established wisdom. Much of the literature on "vertical specialization" (or "fragmentation in the parlance of trade economists[32]) assumes that it results in a shift from "hierarchies" (vertically integrated multinational corporations) to "more reliance on arms-length transactions between firms in different countries" (Jones and Kierzkowski, 2001: 36). For Langlois (2001), vertical specialization implies that the "Visible Hand" of large manufacturing firms will become invisible, enhancing the role of market forces. A key proposition of this literature is that "there is an increasing role to be played by separate firms (perhaps smaller than in the past) connected only by the rules of the international market place." (Jones and Kierzkowski, 2000: 6).

I will demonstrate that this proposition does not hold for chip design. I will first present empirical evidence that contradicts expectations that vertical specialization in chip design will enhance the role of market forces. Next, I place this question in a broader context, examining how the structure and the competitive dynamics of the global semiconductor industry has been transformed by vertical specialization through global production and design networks. I will then explore why GDNs are required to manage multiple design interfaces that reflect the growing complexity of SoC design. Finally, I will look at two enabling forces that are gradually reducing constraints to the diffusion of design knowledge to Asia: ICT-enhanced information

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[32] For example, Feenstra, 1998; Jones and Kierzskowski, 2000; Cheng and Kierzkowski, 2001

management, and transnational knowledge communities that facilitate the exchange of tacit knowledge.
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4.1. Licensing of SIPs

Of critical importance for SoC design is the interface with SIP providers outside the SoC design team. There are three external sources of SIPs (Morris, 2003): (1) in-house SIP libraries that compile building blocks from previous designs; (2) other in-house design teams working in parallel with the main SOC design team; and (3) independent SIP vendors.

During the initial euphoria of the late 1990s, there were widespread expectations that vertical specialization in chip design would lead to a highly fragmented market for SIPs, consisting of small SIP boutique shops. This perception is mirrored in the claim by Linden and Somaya (1993: 545) that "we observe a burgeoning market for licensed DMs (= design modules, or SIPs in industry parlance, DE)". In the conclusions of this article, the authors are struggling to support this claim. Linden and Somaya (2003: 571) state that "integrated modes currently enjoy the upper hand in SoC, primarily due to the initial distribution of industry assets and the lack of supporting licensing institutions at the dawn of the SoC era." They argue however that the balance may shift over time towards open market SIP licensing.

Yet, empirical evidence demonstrates that the exchange of SIPs takes place primarily *within* global system companies and flagship-dominated GDNs (e.g., Martin, 2003:11; Goering, 2002). The global market for SIPs has remained relatively small (**Figure 6**). It consists primarily a few "star" IPs (MPUs, DSPs, memories and analog design blocks), dominated by a handful of specialized global suppliers like ARM, MIPS, Rambus, and DSP Group.

Figure 6: The Global Market for SIPs, 2001

In other words, initial expectations have not materialized that vertical specialization in chip design would lead to a highly fragmented market for SIPs, consisting of small SIP "boutique shops" (Goering, 2002). Instead SIP trade is dominated by a handful of global players. To do so, the flagships of GDNs must have the resources to coordinate, across boundaries, multiple design interfaces, and they must support a global sales force that can provide support services to customers wherever they are located..

In theory, the idea of reusing SIPs looks straightforward. A basic assumption is that the SoC designer (the "user") does not need to understand what drives the operations of the design building blocks that she works with. But in reality, this is often not the case, due to difficulties in defining the data, which obviously defeats the purpose of using SIPs. In the best of worlds (a favorite term of chip designers), the solution would be to talk to the original SIP design team, establishing a person-to-person contact between SIP creators ("block authors") and SIP users (the SoC designers). In the real world of ruthless global competition, this is practically impossible. A global SIP provider like ARM, for instance, is normally supporting a number of clients at the same time, and the SoC team may well be dealing simultaneously with a number of SIP providers.

A second-best approach is that both the SoC team and the SIP provider assign a single contact person (a customer support engineer at the SIP vendor, and an engineering manager on the SoC team) who can establish temporary connections between members of both teams to solve particularly difficult problems. Especially for complex projects, one often finds " team members from one side moving into the other's facility for extended lengths of time." (Wilson 2003: 60). This again shows that proximity advantages continue to matter, even as vertical specialization of design keeps expanding. For design teams, this implies that they need to develop "second-best" management approaches that allow for the selective exploitation of proximity advantages, while

reaping the benefits of vertical specialization. Vertical specialization within GDNs is a new organizational model that attempts to solve this problem.

4.2. Asymmetry: Vertical Specialization in the Global Semiconductor Industry

Progressive vertical specialization has fundamentally transformed the structure and the competitive dynamics of the global semiconductor industry. As shown in **Figure 7**, vertical specialization is simultaneously driven by two main actors, the "global set makers" (or "system companies") that dominate global brands for computing, communication and consumer devices, and the "silicon vendors". The latter is a new term for semiconductor firms that captures their transformation from component suppliers with a core competency in process technology to vendors of silicon systems who increasingly focus on system-level design skills and capabilities.

Figure 7:Vertical Specialization in the IT Industry

Let us first look at the system level. Set makers have first outsourced manufacturing and design implementation services to (mostly US-controlled) electronic manufacturing service providers (EMSs) and, primarily Taiwan-controlled, original-design manufacturing service providers (ODMs) (Sturgeon, 2002; Luthje, 2002; Ernst, 2003 a; Ernst, 2004 b). Set makers are however now also engaged in the outsourcing of higher-end, more knowledge-intensive activities. They routinely source chip design from fabless companies, who have their chips fabricated by "foundries". But set makers also buy in so-called "star" SIPs (i.e MPUs, DSPs, memories and analog design blocks). In some cases, set makers may also source for "design platforms", especially when they either lack sufficient in-house capabilities, or where they are eager to rapidly expand market share.

The other side of the coin is vertical specialization pursued in the semiconductor industry. Competitive strategies in this industry are experiencing a fundamental shift from process technology to system-level design skills and capabilities[33]. Silicon vendors now come in different incarnations. They can be "silicon foundries", i.e. contract manufacturers of given chip designs. They also can be IDMs who, like Intel, keep much of chip design and fabrication in-house. However, the cost of keeping fabrication facilities running, let alone the cost of upgrading them, has risen exponentially. For instance, $ 3 billion and more is the current minimum investment outlay required for state-of-the art 12 inch fabrication plants, and these very high investment thresholds are continuing to rise. As a result, IDMs now cooperate in R&D and jointly build wafer fabs for the production of new chips, in an effort to control costs and risks. Some IDMs are attempting to reduce their exposure to fabrication. By outsourcing fabrication to "silicon foundries", these IDMs have become so-called "fab-lite" firms, a model introduced by Motorola. More recently, vertical specialization has produced two new types of silicon vendors, the so-called SIP providers, and the so-called platform leaders, like Intel. But now also set makers have aggressively entered the market for platform leaders, blurring the erstwhile distinctive boundaries between set makers and silicon vendors.

As a result, silicon vendors are increasingly being transformed into "systems solution providers that also sell the software" (Claasen, 2003: 20) System design and software development are migrating to silicon vendors, who need to shoulder a much higher share of the overall cost of developing electronic systems. As system-level architecture and architectural verification are now becoming an integral part of chip design, this dramatically increases its

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[33] With regard to process technology, most IDMs seem to lag behind the leading foundries, with the exception of IBM and Intel (IBS, 2002: 7). Most IDMs can no longer rely on leading-edge process technology as their main strategic weapon; they need to develop strong system design and platform design capabilities.

complexity. In short, all of these changes in industry structure and firm behavior imply that both set makers and silicon vendors need to rely on vertical specialization through GDNs.

4.3. Managing Multiple Design Interfaces

A good indicator of the growing organizational complexity of SoC design is the variety of design interfaces that need to be managed. An interface is created when information must flow, and when knowledge must be exchanged, "…between groups that are isolated from each other, whether by goals, methodologies, geography or culture" (Wilson, 2003: 49).

This is exactly what is happening with SoC design. The diversity of functions that must be integrated into the chip means that "various blocks within the finished design will have come from different groups, some within and some outside the design team. Some of these groups will not be involved in the chip design process at all, and may not share a vocabulary, or even a language and culture with the primary chip design group." (Wilson, 2003:48). A typical SoC design team needs to manage at least six main types of design interfaces (**Figure 8**): with system designers, with SIP providers, with software developers, with verification teams, with EDA tool vendors, as well as with foundry services (fabrication).

Figure 8: Multiple SOC Design Interfaces

In addition, these different design network communities are spread across the ten *strategic groups* that participate in GDNs that I have described at the beginning of this paper. Managing these multiple design interfaces poses extremely demanding coordination requirements. For instance, each of the different design network communities insists on using their own language and tools. Typically, in SoC design teams, there are "islands of automation" of different design tasks, each based on a different language. Nobody will easily give up the language or the approach used for their own particular task for the sake of the overall flow" (Pierre Bricaud, design manager at Mentor Graphics, quoted in "SoC designers describe their 'best practices'", 2002). Attempts to adjust design tools and practices to overcome such communication gaps are important. But their effect will always depend on the quality of engineers.

At the same time, there are powerful pressures to increase the codification of knowledge. As design teams become larger and geographically dispersed, "…(w)e capture as much as we can in automated flows, which are documented and posted on the web" (Mike Fazeli, design manager at Texas Instruments, quoted in "SoC designers describe their 'best practices'", 2002). To keep the design networks growing, it is necessary to develop more formal interfaces between the different network nodes. Design groups that are separated by distance or design disciplines need to be able to communicate with each other. While they share a common objective, they use highly dissimilar vocabularies. Defining interfaces requires shared definitions of the data that need to be exchanged, of the formats and protocols that govern data transfer and interpretation, and of the economic performance requirements of the designs. Developing a precise common vocabulary for these three interface attributes is extremely difficult. Equally important, data must be translated into a form usable by different design groups. Let us look at two illustrative examples of design interface management within GDNs: with system designers and with foundry services.

By definition, SoC design requires close interaction with *system designers*, marketing people and end customers (the "set makers"). With product life cycles often as short as six months or less, system design requirements keep changing. The protocol necessary to transmit these changes real-time to all the different design network participants is "one of the great unsolved

problems of design management". (Wilson, 2003: 56)[34]. Hence, proximity and face-to-face contact are important. As we have seen, an important new development in Asia is that this region not only provides important growth markets for existing electronic products and services, but also test beds and launch markets for important innovations and global standards in mobile communications and digital consumer electronics. This implies that GDNs need to locate those chip design stages in Asia that strongly interface with Asia-based system designers.

Interactions with foundry services are arguably the most explicitly recognized interfaces in the entire SoC flow, with well documented and automatically checkable "design rules" (Macher, Mowery and Simco, 2002) (**Figure 9)**. Yet, with growing complexity of SoC design, the management of the foundry interface also poses new challenges (Wilson, 2003:62-65). A combination of new processes and drastic changes in design methodology implies that design rules need to be tweaked and stretched, and that process limitations are there "to be explored not worshipped" (Wilson, 2003: 63), requiring a much closer interaction between designers and process engineers. From the perspective of foundries, for instance, sub-micron process technology makes yield enhancement much more difficult for 20 to 50 million transistor SoCs (author's interview with Taiwanese foundry, September 22, 2003).

Figure 9: The Foundry Interfaces

As processes grow more demanding, mask makers and process engineers will try to pass this growing complexity to the chip design team through an enormous increase in complexity in either cell selection or design rules. For instance, a leading-edge SoC design is likely to require 22 separate cells. And the foundry's process engineers now include into the design rules for SoC designers the request to "design-for-yield-enhancement."

This new interface requirement means that design teams must adjust the design to improve the odds that the process will yield well and that the dice will continue working even under demanding system performance requirements. In other words, designers must take into account the effects of fabrication process variations, which makes design even more complex. There is now a much greater need for dense interaction between physical designers and process integration teams, even for relatively stable designs. Designers increasingly must take into account the intricacies of process development. An "extraordinary degree of coordination" is required between SoC designers, mask makers, foundries, and third party SIP suppliers ("90-nm design flow is seen as a community effort", 2003). As the world's leading foundries are all based in Asia (see part 1), this creates powerful pressures for GDNs to relocate increasingly important stages of chip design to this region.

In short, chip design has become itself a highly complex technology system, where multiple communication and knowledge exchange interfaces must be managed simultaneously. While the idea of reusing SIPs is great, its implementation requires a degree of cooperation that was unthinkable even a few years ago. This is true for all the different design interfaces. Ironically, the more SoC design moves into sub-micron territory, the more the pendulum swings back towards a reintegration of design and manufacturing.

This implies that, with the increasing complexity of interactive SoC design systems, geographic dispersion needs to complement reorganization: knowledge exchange must now extend beyond firm boundaries and national borders. SoC design requires a combination of

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[34] Communication is also fraught with problems between hardware and software designers: "Verilog representation of a block by hardware designers, for example, may need to be translated into …. a Java transaction-level model of the block for use by software designers." (Wilson, 2003: 52). The amount of work required for this translation is enormous, so much depends on the availability of new software tools that would make a progressive automation possible.

designers with multiple, highly diverse capabilities. To bring together such a large group of very diverse people at one location, and to keep it there, becomes increasingly costly. When spatially concentrated, such design groups also may become too powerful, and hence may constrain productivity growth. But once they become dispersed, this creates extremely demanding coordination requirements for managing multiple chip design interfaces. Neither complete localization nor complete vertical specialization through a shift to invisible market forces can cope with the challenges that result from increasing design complexity. An alternative is to develop GDNs that provide an efficient and flexible organizational environment for the exchange of design knowledge across diverse design communities that are not co-located.

4.4. The New Mobility of Design Knowledge: Enabling Forces

This brings me to my last question: What explains that GDNs are gradually reducing constraints to the diffusion of relevant design knowledge to Asia? **Figure 10** provides a stylized model of how *vertical specialization* (i.e. the dis-integration of firm organization and the geographic dispersion across national boundaries) and *re-integration* of dispersed production, distribution and innovation bases into hierarchical *global flagship networks* facilitate *knowledge diffusion* (Ernst, 2003b and c). **Figure 10** also demonstrates the role played by two complementary enabling forces in enhancing both codified and tacit knowledge exchange: *ICT-enhanced information management* and *transnational knowledge communities*.

Figure 10: Vertical Specialization, GFNs and Knowledge Diffusion

Let us first look at the latter two enabling factors. In all Asian countries, but especially in China, earlier "brain drain" has produced overseas communities of engineers, scholars, and managers who are familiar with cutting-edge technology and best-practice management approaches and who understand the dynamics of international product and financial markets. These "transnational knowledge communities" can play an important catalytic role in the development of domestic innovative capabilities (Saxenian, 2002).

The use of ICT as a management tool can enhance the scope for knowledge sharing among multiple network participants at distant locations (Ernst, 2003 c). But these changes will occur only gradually, as a long-term, iterative learning process, based on search and experimentation. The digitization of knowledge implies that it can be delivered as a service and built around open standards. This has fostered the specialization of knowledge creation, giving rise to a process of modularization, very much like earlier modularization processes in hardware manufacturing. While this paper has highlighted the substantial implementation problems, it is nevertheless true that the use of ICT-enhanced information management will facilitate the reuse of chip design knowledge through GDNs.

Under the heading of "e-business", a new generation of networking software provides a greater variety of tools for representing knowledge, including low-cost audio-visual representations (Foray and Steinmueller, 2001). Those programs also provide flexible information systems that support not only information exchange among dispersed network nodes, but also the sharing, utilization, and creation of knowledge among multiple network participants at remote locations (Jørgensen and Kogstie, 2000). New forms of remote control are emerging for various design stages, as well as the management of quality, supply chains, and customer relations. Equally important are new opportunities for the joint production, across different time zones, of complex chip designs.

Let us now turn to the characteristics of global flagship networks (the central box in **figure 10)**, of which design networks (GDNs) are just one manifestation, complementing the global production networks (GPNs) that have been around for a much longer time. Trade economists

have recently discovered the importance of changes in the organization of international production as a determinant of trade patterns (for example, Feenstra, 1998; Jones and Kierzskowski, 2000; Cheng and Kierzkowski, 2001). Their work demonstrates that (i) production is increasingly 'fragmented', with parts of the production process being scattered across a number of countries, hence increasing the share of trade in parts and components; (ii) that there is reintegration through global production networks; and (iii) that countries and regions which have been able to become a part of these network are the ones which have industrialized the fastest.

The model of GFNs builds on this work, but uses a broader concept that emphasizes three essential characteristics (Ernst, 2002a, 2002 b, 2003c): i) *scope*: GFNs encompass all stages of the value chain, not just production; ii) *asymmetry*: flagships dominate control over network resources and decision-making; and iii) *knowledge diffusion*: global corporations (the "network flagships") construct these networks to gain quick access to skills and capabilities at lower-cost overseas locations that complement their core competencies. Flagships need to transfer technical and managerial knowledge to local suppliers to ensure that they meet the technical specifications mandated by the flagships. Originally this involved primarily operational skills and routine procedures required for sales and distribution, manufacturing and logistics. Over time, knowledge sharing also incorporates higher-level, mostly tacit forms of "organizational knowledge" required for control, coordination, planning and decision-making, as well as for learning and innovation (Ernst and Kim, 2002).

Our research indicates that similar, albeit more complex mechanisms might be at work in global design networks. These networks integrate geographically dispersed companies that are contributing to the complete solution of a particular chip design project. The main purpose of GDNs is to facilitate the reuse of design building blocks, the so-called "silicon intellectual properties" (SIPs). Hence, knowledge-sharing is the glue that keeps these networks growing, facilitating the relocation of chip design to Asia.

Conclusions

This paper has explored why chip design is moving to Asia, despite its high knowledge intensity. A central proposition is that Pavitt's conceptualization of cognitive and organizational complexity can help to explain what forces are behind the growing geographic mobility of chip design, pushing for and enabling its dispersion to Asia. These "push" factors need to complement an analysis of "pull" factors, i.e. differences in the cost of employing a chip design engineer across locations that result from comparative factor and resource advantages, and from support policies that provide incentives and "public goods". Pull factors are important - they explain what attracts chip design to particular locations. But they cannot explain under what conditions physical proximity can become a disadvantage rather than an advantage for innovative activities that involve highly complex technological knowledge.

To address this puzzling question, the paper has analyzed how radical changes in methodology ("system-level integration" through "modular design") and organization (automated "design factory"*)* affect the geographic location of chip design. Both changes have been introduced to improve design productivity and to cope with the growing complexity at two levels of chip design: "silicon complexity", i.e. malfunctions that result from the growing scale and density of the circuit and the introduction of new materials or design architectures; and "system complexity" that increases with the transition to system-level design with "exploding" multiple performance requirements. I show that *de facto* impacts fail to match with expectations: both changes in methodology and organization have further increased the cognitive and organizational complexity of design.

The paper reviews attempts to adjust the organization of design, so that the new methodologies can produce the expected results. I show that *integrated* forms of design organization, where (almost) entire integrated circuits (ICs) are designed within a single firm, are giving way to *vertical specialization* where stages of chip design are outsourced to other firms (*dis-integration of firm organization*) and relocated across national boundaries (*geographic dispersion*). The paper emphasizes that far-reaching changes are required in skill requirements and work organization to reduce the resistance to the new methodology and organization of design. As this resistance is greater in industrialized countries than in Asia, this provides an additional powerful incentive for relocating chip design to new lower-cost locations in Asia.

It is important to emphasize that these findings add an important qualification to a widely accepted proposition that, as relevant knowledge can now be codified in frameworks and categories, codification will "naturally" enhance the division of innovative labor by lowering the transaction cost of technological knowledge (e.g., Arora and Gambardella, 1994). As Tokumaru (2004: 3) observes, this concept of "knowledge" comes very close to Arrow's (1962) concept of context-independent information that can be easily transmitted. By reducing learning to information processing, that proposition neglects the increasing complexity of technological knowledge that accompanies the process of codification, as this paper demonstrates for chip design.

The paper also adds a second important qualification to the study of internationalization of innovation. I emphasize that vertical specialization does not imply that the "Visible Hand" of large global corporations will become invisible (as argued, for instance, in Langlois, 2001), giving rise to a resurgence of market forces. In line with Pavitt (2003a and 2003 b), Brusoni (2003), Tokumaru (2004) , and Brusoni, Prencipe and Pavitt (2001), this paper introduces a counter-proposition: if codification does not reduce complexity (which it fails to do in chip design), then the division of innovative labor will remain constrained, and requires more (not less) coordination through system integrators or network flagships. This confirms Brusoni's (2003:11) observation that firms "are not replaced by markets, but by the temporary hierarchy defined within a specific project". For each specific project, for instance the design of an embedded micro-controller for a mobile phone for Motorola, the global design network (GDN) "provides a temporary administrative framework within which some form of hierarchical coordination replaces the market." (ibid: 15)

Based on interviews with a representative sample of strategic groups of firms that together shape the development of chip design, I show that network integration is the necessary complement to vertical specialization. Global corporations (the "network flagships") integrate geographically dispersed companies (the "network suppliers") that are contributing to the complete solution of a particular chip design project into hierarchical GDNs. Vertical specialization increases the number and variety of network participants, as well as the variety of business models, which in turn increases the organizational complexity of these networks. I show that this growing organizational complexity gives rise to multiple design interfaces that pose very demanding coordination requirements. For each SoC design project, a design team needs to manage at least six main types of design interfaces: with system designers, with SIP providers, with software developers, with verification teams, with EDA tool vendors, as well as with foundry services (fabrication).

I show that, in order to cope with the growing complexity of chip design, GDNs are *asymmetric*: flagships dominate control over network resources and decision-making. This implies that these networks do not necessarily give rise to less hierarchical forms of firm organization (as predicted, for instance, in Bartlett and Ghoshal, 1989, and in Nohria and Eccles, 1992). GDNs typically consist of various hierarchical layers, ranging from network flagships that dominate such networks, due to their capacity for system integration (Pavitt, 2003 b), down to a

variety of usually smaller, local specialized network suppliers. Vertical specialization within geographically dispersed GDNs requires system integrators who are able to frame problems (system architecture and design building blocks or SIPs) by identifying and "freezing" the crucial technological and organizational interdependencies. Global design network flagships thus need to retain diversified technology bases ("design libraries") in order to coordinate the development of the underlying knowledge bases[35].

But GDNs cannot work without quite extensive sharing of knowledge. This is necessary in order to upgrade the suppliers` capabilities, so that they can meet the technical specifications of the flagships. In line with Rugman and D'Cruz (2000), we find that the hierarchical nature of design networks apparently facilitates knowledge transfer. Their asymmetric distribution of resources, power and decision-making can facilitate trust and credible commitments, enhancing stability, coherence and organizational learning. This reduces the risks that flagships encounter when sharing technology.

The paper highlights two enabling forces that are gradually reducing constraints to the diffusion of design knowledge to Asia: ICT-enhanced information management, and the integration of geographically dispersed design communities (the "transnational knowledge communities"). GDNs expand inter-firm linkages across national boundaries, increasing the need for knowledge diffusion. ICT-enhanced information management provides not only new opportunities for information exchange, but also for the sharing and joint creation of knowledge. Finally, transnational knowledge communities add the critically important missing link: they facilitate the exchange of tacit knowledge that is necessary to cope with growing design complexity. It is this new mobility of knowledge that explains why chip design is moving to Asia, despite its high knowledge intensity.

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[35] This confirms the findings of Granstrand, Patel, and Pavitt (1997) that large firms are more diversified in the technologies they master than the products that they make and that their technological diversity has been increasing while typically their product range has narrowed.

APPENDIX (Figures 1 - 10)

Figure 1.

Taiwan's Competitive Advantages in Circuit Design
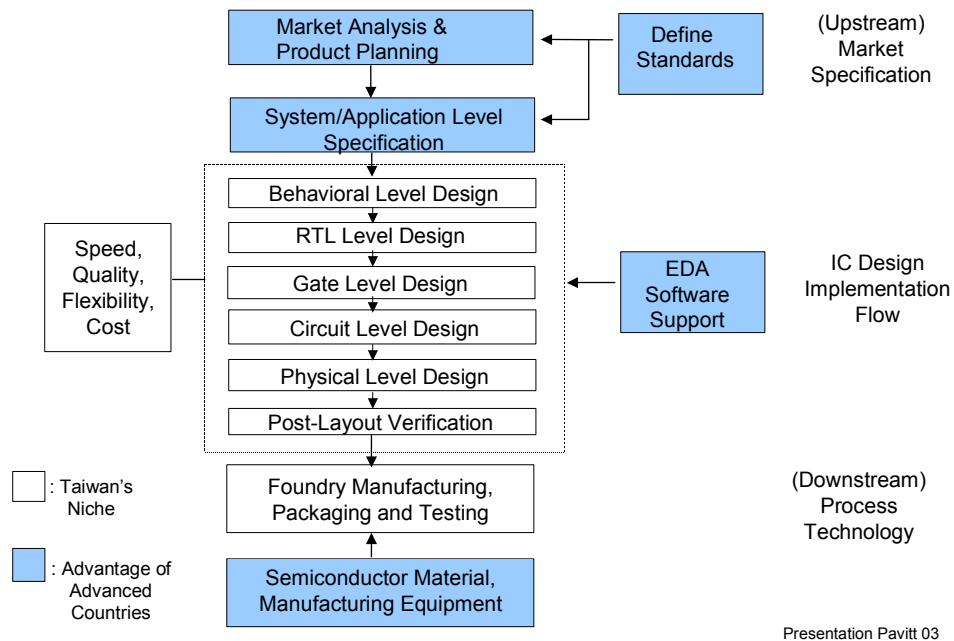
Source: Chang and Tsai, 2002

Figure 2.

**Annual Cost of Employing a
Chip Design Engineer* (US-$), 2002**

Location	Annual Cost
Silicon Valley	300,000
Canada	150,000
Ireland	75,000
Taiwan	<60,000
South Korea	<65,000
China	28,000 (Shanghai)
	24,000 (Suzhou)
India	30,000

*= including salary, benefits, equipment, office space and other infrastructure.
Sources: PMC-Sierra Inc, Burnaby, Canada (for Silicon Valley, Canada, Ireland, India);
plus interviews (Taiwan, South Korea, China)

Figure 3.

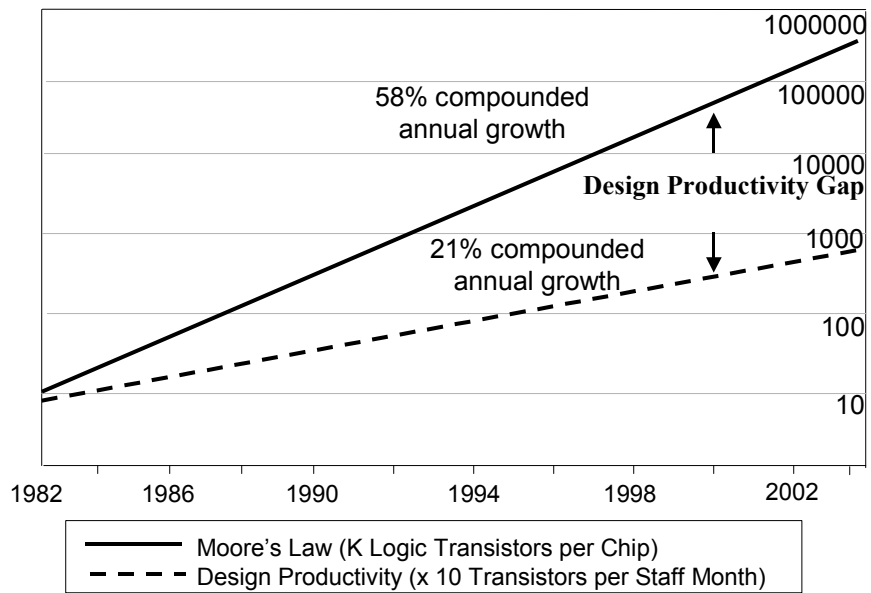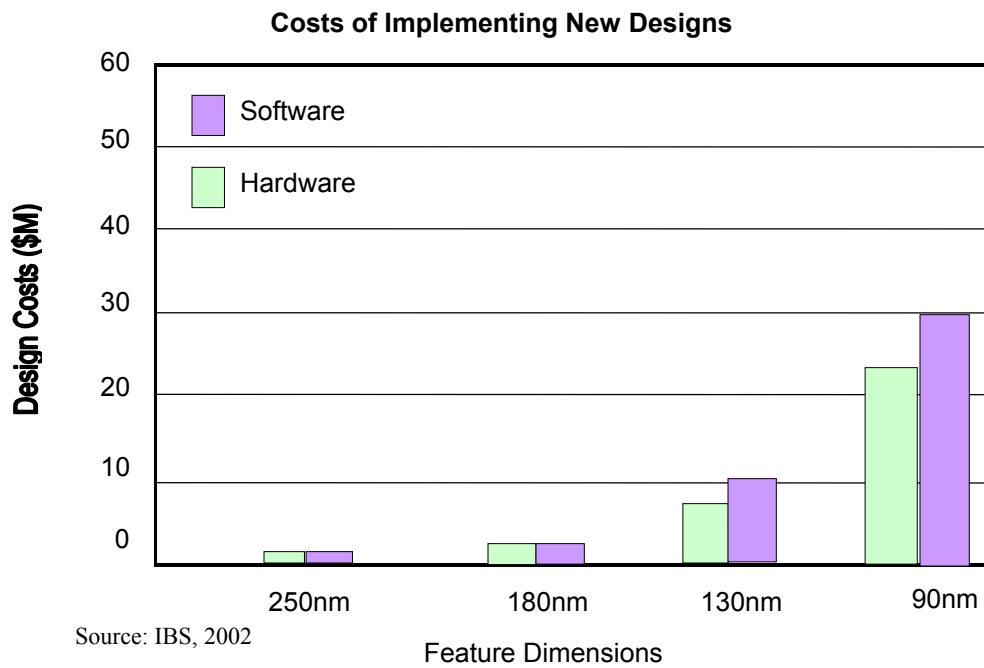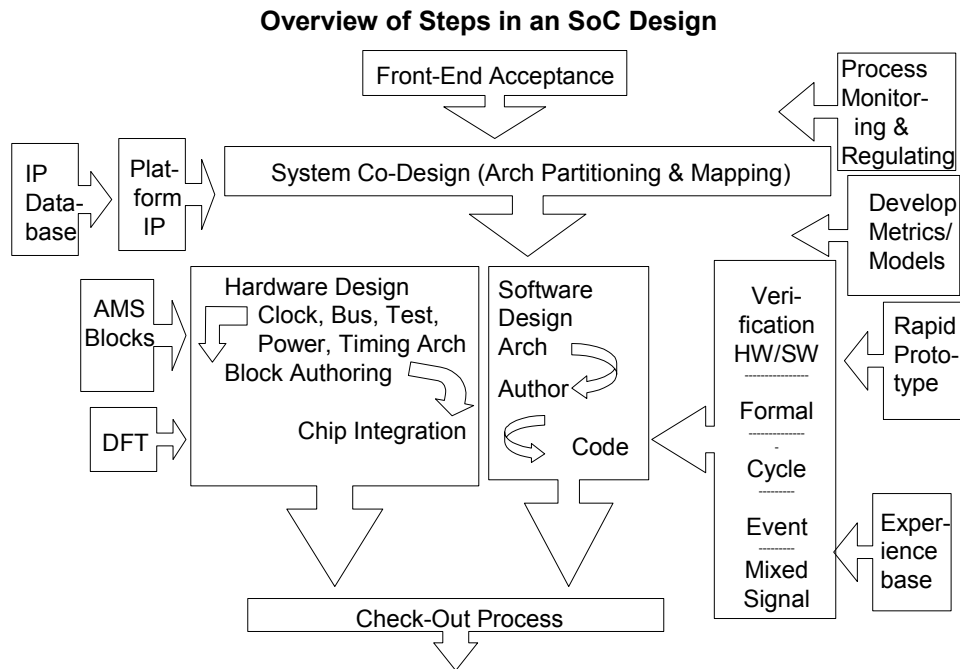### Widening Design Productivity Gap in Integrated Circuits

Moore's Law (K Logic Transistors per Chip)
Design Productivity (x 10 Transistors per Staff Month)

Figure 4.

Costs of Implementing New Designs

Source: IBS, 2002

Figure 5.

Overview of Steps in an SoC Design

Source: Martin 2003

Figure 6.

The Global Market for SIPs, 2001, US
(% shares)

"star" SIPs (MPUs, DSPs, memories; analog design blocks)	778
"commodity" SIPs	114
SIPs , total	892
IC market, total	121,302
share of SIP market in total IC market	(0.735)

Source: Dataquest, 2002

Figure 7.
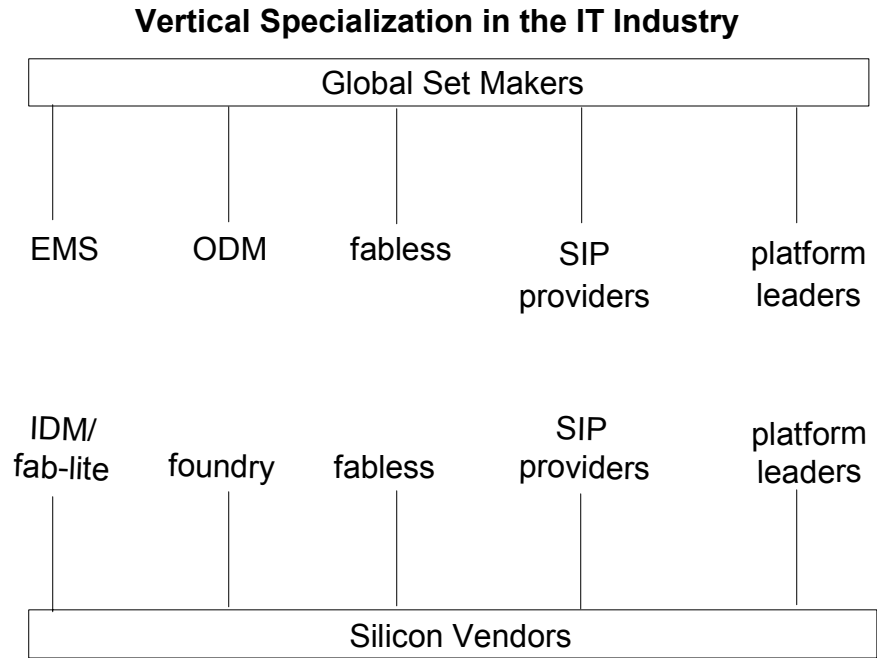
Vertical Specialization in the IT Industry

Global Set Makers

EMS   ODM   fabless   SIP providers   platform leaders

IDM/ fab-lite   foundry   fabless   SIP providers   platform leaders

Silicon Vendors

Figure 8.

Multiple SOC Design Interfaces

foundry services

system designers

EDA tool vendors

SOC Design Teams

SIP providers

verification teams

software developers

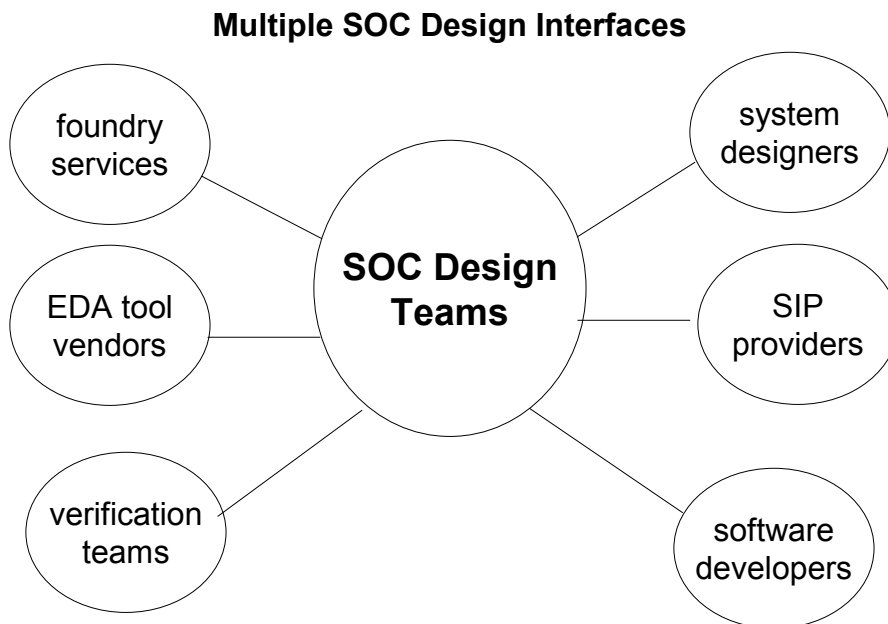Source: Morris, 2003

Figure 9.

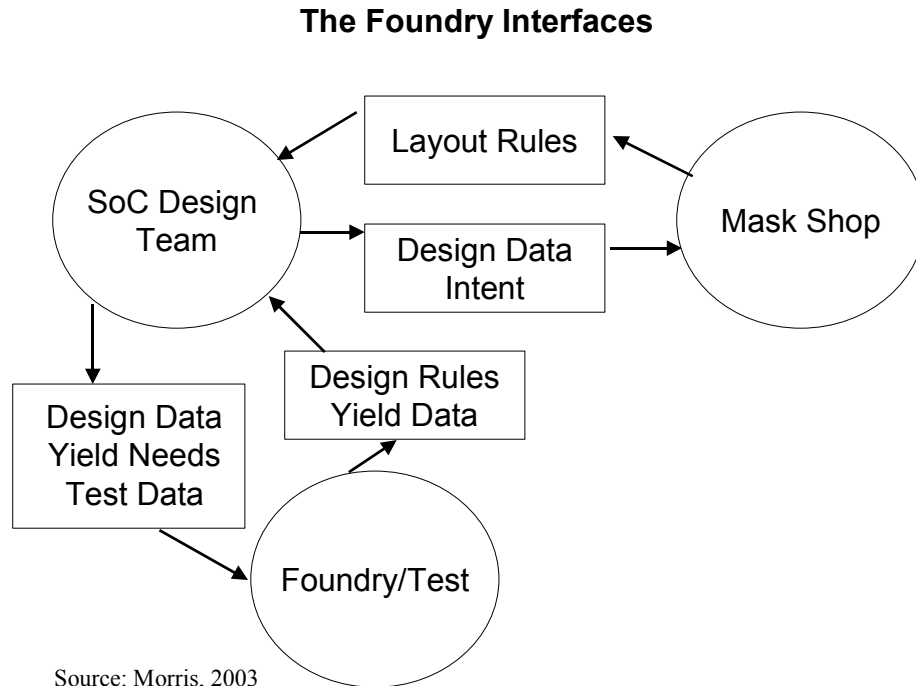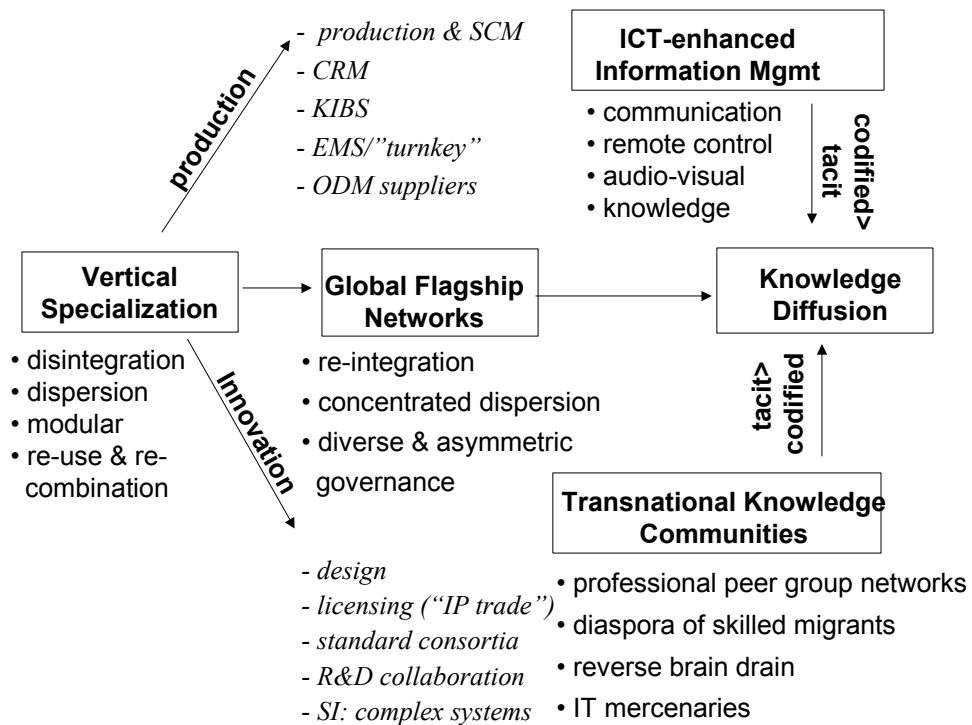### The Foundry Interfaces

Source: Morris, 2003

Figure 10. **Vertical Specialization, GFNs, and Knowledge Diffusion**

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